

The Royal Academy of Engineering

Research Fellowship

Power-Aware Compilation in a Multi-core Era

Co-funded by EPSRC

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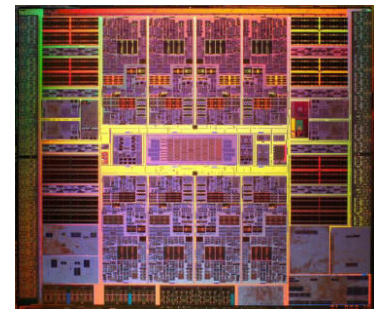
School of Informatics, University of Edinburgh



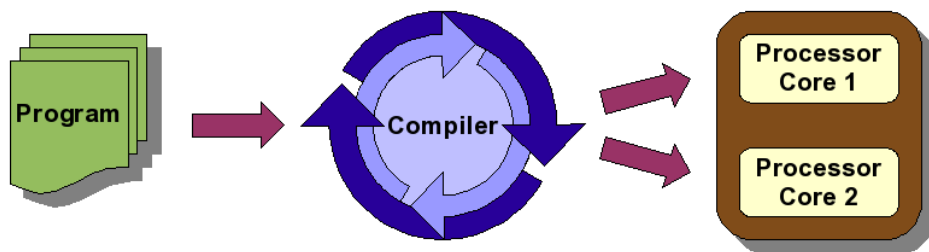
Overview

The computer world has gone multi-core. Manufacturers are putting two or more processor cores on one chip to extract as much performance as possible from the transistors available to them. However, unless managed efficiently, these cores can consume significant amounts of energy. This gets converted into heat and must be extracted from the system using costly cooling schemes.

Techniques that can reduce the amount of energy consumed by the processor will save money during design and manufacture, leading to higher performance computers. For the end user, this means more powerful systems, cheaper devices and longer battery lives.



Compilation



My fellowship seeks to address this through the use of the compiler. The compiler is a piece of software that converts a program from a human-readable format into the 1s and 0s that run on the actual processor. Along the way it performs analyses and transformations to make the final program run as optimally as possible.

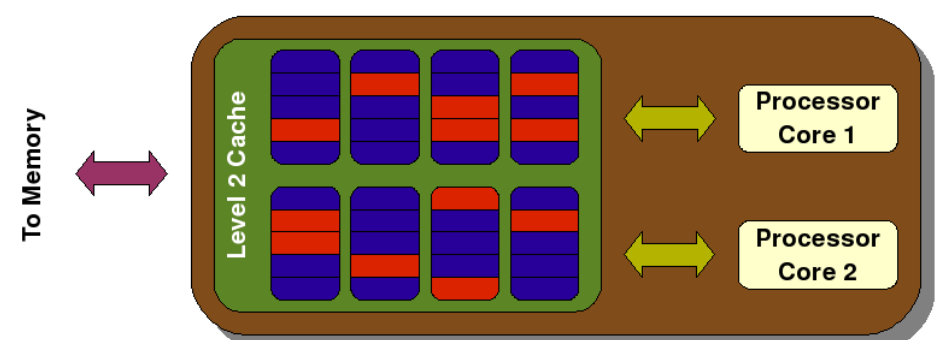
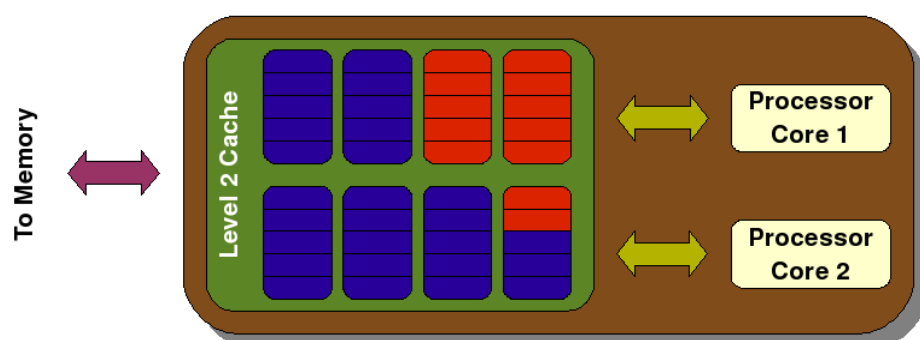
Current Work

The memory hierarchy is a critical component of any processor. Multiple levels of cache are used to store data close to the processor for fast access. However, caches account for well over half the area of a modern high-performance processor, so it is important to keep their energy footprint low.

to see if it contains the required data. However, if the same bank is repeatedly accessed, its temperature will rise due to the electrical energy consumed each time.

Caches are organised as a group of banks, each containing a portion of the data being stored. On an access to the cache, only one of the banks is consulted

Current research is looking at how to organise program data so that accesses are spread evenly amongst all banks. The compiler estimates which data will be required at any given point in the program. Using this knowledge it can place the data in memory at positions that will map to different banks within the cache.



The Fellowship

The aim of my fellowship is to develop energy-saving features at three key stages in the system's life cycle: at

design of compiler and processor; during compilation; and when executing programs on the final system.